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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/420,086	10/18/1999	WARREN M. FARNWORTH	98-0105.01	2322

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EXAMINER	
PAREKH, NITIN	

ART UNIT	PAPER NUMBER
2811	

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/420,086	FARNWORTH ET AL.	
	Examiner	Art Unit	
	Nitin Parekh	2811	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *12 January 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *25-39 and 47-53* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *25-39 and 47-53* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *10-18-1999* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 25, 26, 28-33, 35-37, 39, 47, 48 and 51-53 are rejected under 35 U.S.C. 103(a) as being unpatentable over Chou et al. (US Pat. 5691568).

Regarding clam 25, Chou et al. disclose a semiconductor component/assembly/package (1000 in Fig. 10A/10B; Col. 16, lines 5-21) comprising:

- a substrate made of material such as a printed circuit board (PCB), plastic/epoxy laminate, ceramic, etc. (not numerically referenced in Fig. 10A/10B- Col. 1, line 53, Col. 10, line 29, Col. 16, line 46) having top and bottom surfaces
- a conductive layer comprising a metal conductive layer (512/1011a-1011d in Fig. 10A/10B; Col. 10, lines 30-53) having elements/land segments comprising a plurality of first portions (1011a and 1011d in Fig. 10A/10B) and a plurality of second portions (1011b, 1011c and 512 in Fig. 10A/10B)
- a plurality of conductors on the first and second portions comprising conductive pads/sites (not numerically referenced- see bonding pads/sites on 1011a, 1011b, etc. connected by bonding wires in Fig. 10A), those on the first portions being

separated and electrically isolated from one another by those on the second portions of the conductive layer (see 1011a/1011d being spaced from 101 lb in Fig. 10A/10B)

- a plurality of recesses/grooves (not numerically referenced- see recesses/grooves having predetermined size, shape and width in Fig. 10A/10B between the conductive portions of the conductive layer) in the conductive layer defining a size, a spacing and a shape (Col. 11, lines 20-24) of the conductors and the second portions of the conductive layer

- a semiconductor die (die 502 in Fig. 10A/10B) on the top surface of the substrate in an electrical communication with the conductors comprising conductive portions/conductive pads

- a plurality of electrically conductive vias through the substrate (1034a, 1034b, etc. in Fig. 10A/10B) in electrical communication with the conductors/conductive pads (1011a, 101 lb, etc. respectively in Fig. 10A), and

- a plurality of external contacts/balls (not numerically referenced in Fig. 10A- see 522a-522e in Fig. 5B; Col.16, lines 46-53) in a ball grid array (BGA) on the bottom surface of the substrate, the external contacts/balls being in electrical communication with the respective conductive vias and conductive portions of the conducive layer (Col. 16, lines 33-38)

(Fig. 10A/10B; Fig. 5A-5G; Col. 16, line 5- Col. 17, line 15).

Chou et al. fail to teach the conductive metal layer substantially covering the surface of the substrate and the plurality of first and second portions of the conductive layer being configured for signal transmission and non-signal transmission respectively.

Chou et al. further teach in another embodiment (Fig. 11A/11B), the conductive layer being extended to include a thermally and an electrically conductive die attach/paddle metal area (Col. 17, lines 16-50), the die attach/paddle metal area being selectively connected with one or more of the land segment/pad region of the first or second portions of the conductive layer to provide a significant increase in the area covering the surface of the substrate and to provide the enhanced thermal dissipation and heat transfer from the die (Col. 17, lines 50-65). Furthermore, such land/pad connections comprise one or more grounded/non-signal transmission electrical connections (see Col. 17, lines 30-50).

It would have been obvious to a person of ordinary skill in the art at the time invention was made to incorporate the conductive metal layer substantially covering the surface of the substrate and the plurality of first and second portions of the conductive layer being configured for signal transmission and non-signal respectively as taught by Chou et al. in the embodiment of Fig. 11A/11B so that the thermal dissipation and electrical performance/grounding can be improved in Chou et al's component.

Regarding claim 25, forming the elements do not distinguish over Chou et al. because only the final product/structure is relevant, not the process of forming the elements such as "photo processing/etching", "laser machining", "drilling" or "plasma processing". Note that a "product by process" claim is directed to the product per se, no matter how actually made, In re Hirao, 190 USPQ 15 at 17 (footnote 3). See also In re Brown, 173 USPQ 685; In re Luck, 177 USPQ 523; In re Fessmann, 180 USPQ 324; In re Avery, 186 USPQ 161; In re Wertheim, 191 USPQ 90 (209 USPQ 554 does not deal with this issue); and In re Marrosi et al., 218 USPQ 289, all of which make it clear that it is the patentability of the final product per se which must be determined in a "product by process" claim, and not the patentability of the process, and that an old or obvious product produced by a new method is not patentable as a product, whether claimed in "product by process" claims or not . Note that applicant has the burden of proof in such cases, as the above case law makes clear. See also MPEP 706.03(e).

Regarding claim 26, Chou et al. teach substantially the entire claimed structure as applied to claim 25, wherein Chou et al. teach the semiconductor die being wire bonded to the respective plurality of conductive pads/sites on the conductors (see wire bonds 1026a, 1026b, etc. in Fig. 10A).

Regarding claim 28, Chou et al. teach substantially the entire claimed structure as applied to claim 25, wherein Chou et al. teach the substrate (not numerically referenced

in Fig. 10A/10B; Col. 10, line 29, see 504 in Fig. 5A) comprising a material including plastic or ceramic (Col. 1, line 53, Col. 16, line 46).

Regarding claim 29, Chou et al. teach substantially the entire claimed structure as applied to claim 25, wherein Chou et al. teach the conductors comprising the plurality of external contacts/balls (not numerically referenced in Fig. 10A- see 522a, 522b, etc. in Fig. 5B; Col. 10, lines 35-40, Col.16, lines 46-53) being adapted/adaptable for the electrical connection to the external/outside circuitry.

Regarding claim 30, Chou et al. disclose a semiconductor component/assembly/package (1000 in Fig. 10A/10B, Col. 16, lines 5-21) comprising:
- a substrate made of material such as a printed circuit board (PCB), plastic/epoxy laminate, ceramic, etc. (not numerically referenced in Fig. 10A/10B- Col. 1, line 53, Col. 10, line 29., Col. 16, line 46) having top and bottom surfaces
- a conductive layer comprising a metal conductive layer (512/1011a-1011d in Fig. 10A/10B; Col. 10, lines 30-53) having elements/land segments comprising a plurality of conductors (1011a, 1011b, etc. in Fig. 10A/10B), the conductive layer comprising a metal layer/foil (Col. 10, lines 35-38) being attached/disposed on the top surface of the substrate
- the plurality of conductors having respective conductive pads/sites (see bonding pads/sites on 1011a, 1011b, etc. connected by bonding wires in Fig. 10A) for

electrical connections

- a plurality of recesses/grooves (not numerically referenced- see recesses/grooves between the conductors in Fig. 10A/10B) in the metal layer/foil defining a size, a spacing and a shape (Col. 11, lines 20-24) of the conductors, each conductor being defined by a groove/recess having portions of the metal layer/foil on either side, each portions being separated and electrically isolated from one another (see 1011b being separated by the groove/recess and having 1011a and 1011d on both sides in Fig. 10A/10B),

- a semiconductor die (die 502 in Fig. 10A/10B) being wire bonded to the top surface of the substrate in an electrical communication with the conductors/conductive pads

- a plurality of electrically conductive vias through the substrate (1034a, 1034b, etc. in Fig. 10A/10B) in electrical communication with the conductors (1011a, 1011b, etc. respectively in Fig. 10A) and

- a plurality of external contacts/balls (not numerically referenced in Fig. 10A- see 522a-522e in Fig. 5B; Col.16, lines 46-53) in a ball grid array (BGA) on the bottom surface of the substrate, the external contacts/balls being in electrical communication with the respective conductive vias and conductive portions of the conducive layer (Col. 16, lines 33-38)

(Fig. 10A/10B, Fig. 5A-5G; Col. 16, line 5- Col. 17, line 15).

Chou et al. fail to teach the conductive layer substantially covering the surface of the substrate and the portions of the conductive layer being configured for signal transmission and the remaining portions being configured for non-signal transmission.

Chou et al. further teach in another embodiment (Fig. 11A/11B), the conductive layer being extended to include a thermally and an electrically conductive die attach/paddle metal area (Col. 17, lines 16-50), the die attach/paddle metal area being selectively connected with one or more of the land segment/pad region of the conductive layer to provide a significant increase in the area covering the surface of the substrate and to provide the enhanced thermal dissipation and heat transfer from the die (Col. 17, lines 50-65). Furthermore, such land/pad connection portions comprise one or more grounded/non-signal transmission electrical connections (see Col. 17, lines 30-50).

It would have been obvious to a person of ordinary skill in the art at the time invention was made to incorporate the conductive layer substantially covering the surface of the substrate and the portions of the conductive layer being configured for signal transmission and the remaining portions being configured for non-signal transmission as taught by Chou et al. in the embodiment of Fig. 11A/11B so that the thermal dissipation and electrical performance/grounding can be improved in Chou et al's component.

Regarding claim 30, forming the elements do not distinguish over Chou et al. because only the final product/structure is relevant, not the process of forming the elements such as "photo processing/etching", "laser machining", "drilling" or "plasma processing". Note that a "product by process" claim is directed to the product per se, no matter how actually made, In re Hirao, 190 USPQ 15 at 17 (footnote 3). See also In re Brown, 173 USPQ 685; In re Luck, 177 USPQ 523; In re Fessmann, 180 USPQ 324; In re Avery, 186 USPQ 161; In re Wertheim, 191 USPQ 90 (209 USPQ 554 does not deal with this issue); and In re Marrosi et al.; 218 USPQ 289, all of which make it clear that it is the patentability of the final product per se which must be determined in a "product by process" claim, and not the patentability of the process, and that an old or obvious product produced by a new method is not patentable as a product, whether claimed in "product by process" claims or not . Note that applicant has the burden of proof in such cases, as the above case law makes clear. See also MPEP 706.03(e).

Regarding claim 31 , Chou et al. teach substantially the entire claimed structure as applied to claim 30, wherein Chou et al. teach the conductors comprising the plurality of external contacts/balls (not numerically referenced in Fig. 10A- see 522a, 522b, etc. in Fig. 5B; Col. 10, lines 35-40., Col.16, lines 46-53) being adapted/adaptable for the electrical connection to the external/outside circuitry.

Regarding claim 32, Chou et al. teach substantially the entire claimed structure as applied to claim 30, wherein Chou et al. teach the plurality of conductive vias through the substrate (1034a, 1034b, etc. in Fig. 10A/10B) in electrical communication with the respective conductors (1011a, 1011b, etc. respectively in Fig. 10A) and the plurality of external contacts/contact balls (not numerically referenced in Fig. 10A- see 522 a-522e in Fig. 5B; Col.16, lines 46-53) on the bottom/second surface of the substrate.

Regarding claim 33, Chou et al. teach substantially the entire claimed structure as applied to claim 30, wherein Chou et al. teach the component comprising the assembly/package (1000 in Fig. 10A/10B; Col. 16, line 39).

Regarding claim 35, Chou et al. disclose a semiconductor component/assembly/package (1000 in Fig. 10A/10B; Col. 16, lines 5-21) comprising:
- a substrate made of material such as a printed circuit board (PCB), plastic/epoxy laminate, ceramic, etc. (not numerically referenced in Fig. 10A/10B- Col. 1, line 53, Col. 10, line 29, Col. 16, line 46) having top and bottom surfaces
- a conductive layer (512/1011a-1011d in Fig. 10A/10B) having elements/land segments comprising a plurality of first portions (1011a and 1011d in Fig. 10A/10B) and a plurality of second portions (1011b and 1011c in Fig. 10A/10B)
- a plurality of conductors comprising conductive pads/sites (not numerically referenced- see bonding pads/sites on 1011a, 1011b, etc. connected by bonding

wires in Fig. 10A) on the first portions of the conductive layer being separated and electrically isolated from one another by the second portions of the conductive layer (see 1011a/1011d being spaced from 1011b by a recess/groove in Fig. 10A/10B)

- a plurality of recesses/grooves (not numerically referenced- see recesses/grooves in Fig. 10A/10B) in the conductive layer defining a size, a spacing, a shape and side edges of the conductors (see vertical edges of 1011a, 101 lb, etc. in Fig. 10A, Col. 11 , lines 20-24),

- each conductor being defined by a pair of grooves/recesses and being separated from the adjacent conductor portions, each adjacent first portions of the conductive layer being separated by the second portions of the conductor (see 1011d and 1011 having the edges defined by the grooves/recesses

- a semiconductor die (die 502 in Fig. 10A/10B) being wire bonded to the top surface of the substrate in an electrical communication with the conductors comprising conductive portions

- a plurality of electrically conductive vias through the substrate (1034a, 1034b, etc. in Fig. 10A/10B) in electrical communication with the conductors (1011a, 101 lb, etc. respectively in Fig. 10A), and

-a plurality of external contacts/balls (not numerically referenced in Fig. 10A- see 522a-522e in Fig. 5B; Col.16, lines 46-53) in a ball grid array (BGA) on the bottom surface of the substrate, the external contacts/balls being in electrical

communication with the respective conductive vias and conductive portions of the conducive layer (Col. 16, lines 33-38)
(Fig. 10A/10B; Fig. 5A-5G; Col. 16, line 5- Col. 17, line 15).

Chou et al. fail to teach the conductive metal layer substantially covering the surface of the substrate and the plurality of first and second portions of the conductive layer being configured for signal transmission and non-signal transmission respectively.

Chou et al. further teach in another embodiment (Fig. 11A/11B), the conductive layer being extended to include a thermally and an electrically conductive die attach/paddle metal area (Col. 17, lines 16-50), the die attach/paddle metal area being selectively connected with one or more of the land segment/pad region of the first or second portions of the conductive layer to provide a significant increase in the area covering the surface of the substrate and to provide the enhanced thermal dissipation and heat transfer from the die (Col. 17, lines 50-65). Furthermore, such land/pad connections comprise one or more grounded/non-signal transmission electrical connections (see Col. 17, lines 30-50).

It would have been obvious to a person of ordinary skill in the art at the time invention was made to incorporate the conductive metal layer substantially covering the surface of the substrate and the plurality of first and second portions of the conductive layer being configured for signal transmission and non-signal respectively as taught by Chou et al. in the embodiment of Fig. 11A/11B so that the thermal dissipation and

electrical performance/grounding can be improved in Chou et al's component. Chou et al. fail to teach the conductive layer substantially covering the surface of the substrate.

Regarding claim 35, forming the elements do not distinguish over Chou et al. because only the final product/structure is relevant, not the process of forming the elements such as "photo processing/etching", "laser machining", "drilling" or "plasma processing". Note that a "product by process" claim is directed to the product per se, no matter how actually made, In re Hirao, 190 USPQ 15 at 17 (footnote 3). See also In re Brown, 173 USPQ 685; In re Luck, 177 USPQ 523; In re Fessmann, 180 USPQ 324; In re Avery, 186 USPQ 161; In re Wertheim, 191 USPQ 90 (209 USPQ 554 does not deal with this issue); and In re Marrosi et al., 218 USPQ 289, all of which make it clear that it is the patentability of the final product per se which must be determined in a "product by process" claim, and not the patentability of the process, and that an old or obvious product produced by a new method is not patentable as a product, whether claimed in "product by process" claims or not . Note that applicant has the burden of proof in such cases, as the above case law makes clear. See also MPEP 706.03(e).

Regarding claim 36, Chou et al. teach substantially the entire claimed structure as applied to claim 35, wherein Chou et al. teach the semiconductor die being wire bonded to the respective plurality of conductive pads/sites on the conductive portions (see wire

bonds 1026a, 1026b, etc. in Fig. 10A).

Regarding claim 37, Chou et al. teach substantially the entire claimed structure as applied to claim 35, wherein Chou et al. teach the plurality of conductive pads/sites being wire bonded to the die (see wire bonds 1026a, 1026b, etc. bonding the conductors to respective pads on the die in Fig. 10A) and the plurality of external contacts/balls (not numerically referenced in Fig. 10A- see 522a, 522b, etc. in Fig. 5B; Col. 10, lines 35-40, Col.16, lines 46-53) being adapted/adaptable for the electrical connection to the external/outside circuitry.

Regarding claim 39, Chou et al. teach substantially the entire claimed structure as applied to claim 35, wherein Chou et al. teach the substrate (not numerically referenced in Fig. 10A/10B) comprising the material including plastic or ceramic (Col. 1, line 53, Col. 10, line 29, Col. 16, line 46).

Regarding claim 47, Chou et al. disclose a semiconductor component/assembly/package (1000 in Fig. 10A/10B; Col. 16, lines 5-21) comprising:
- a substrate made of material such as a printed circuit board (PCB), plastic/epoxy laminate, ceramic, etc. (not numerically referenced in Fig. 10A/10B- Col. 1, line 53, Col. 10, line 29., Col. 16, line 46) having top and bottom surfaces
- a conductive layer (512/1011a-1011d in Fig. 10A/10B) comprising a plurality of

portions/elements (1011a, 1011b, 1011c, etc. in Fig. 10A/10B), the conductive portions having a plurality of respective conductors comprising conductive pads/sites (see bonding pads/sites on 1011a, 1011b, etc. connected by bonding wires in Fig. 10A) for electrical connections

- a plurality of recesses/grooves (not numerically referenced- see recesses/grooves in Fig. 10A/10B) in the conductive layer defining a size, a spacing and a shape (Col. 11, lines 20-24) of the conductors, each conductor having opposing edges (see vertical edges of 1011a-1011d in Fig. 10A) being defined by a pair of grooves/recesses (see the pair of grooves/recesses on both sides of 1011a-1011d in Fig. 10A) and each conductor having the portions of the conductive layer on either side being separated from the opposing edges by the pair of grooves/recesses

- a semiconductor die (die 502 in Fig. 10A/10B) being wire bonded on the top surface of the substrate in an electrical communication with the conductors/conductive pads

- a plurality of electrically conductive vias through the substrate (1034a, 1034b, etc. in Fig. 10A/10B) in electrical communication with the conductors (1011a, 1011lb, etc. respectively in Fig. 10A) and

- a plurality of external contacts/balls (not numerically referenced in Fig. 10A- see 522a-522e in Fig. 5B; Col.16, lines 46-53) in a ball grid array (BGA) on the bottom surface of the substrate, the external contacts/balls being in electrical

communication with the respective conductive vias and conductive portions of the conductive layer (Col. 16, lines 33-38)
(Fig. 10A/10B, Fig. 5A-5G; Col. 16, line 5- Col. 17, line 15).

Chou et al. fail to teach the conductive layer substantially covering the surface of the substrate and the portions of the conductive layer being configured for signal transmission and the remaining portions being configured for non-signal transmission respectively.

Chou et al. further teach in another embodiment (Fig. 11A/11B), the conductive layer being extended to include a thermally and an electrically conductive die attach/paddle metal area (Col. 17, lines 16-50), the die attach/paddle metal area being selectively connected with one or more of the land segment/pad region of the conductive layer to provide a significant increase in the area covering the surface of the substrate and to provide the enhanced thermal dissipation and heat transfer from the die (Col. 17, lines 50-65). Furthermore, such land/pad connection portions comprise one or more grounded/non-signal transmission electrical connections (see Col. 17, lines 30-50).

It would have been obvious to a person of ordinary skill in the art at the time invention was made to incorporate the conductive layer substantially covering the surface of the substrate and the portions of the conductive layer being configured for signal transmission and the remaining portions being configured for non-signal

transmission respectively as taught by Chou et al. in the embodiment of Fig. 11A/11B so that the thermal dissipation and electrical performance/grounding can be improved in Chou et al's component.

Regarding claim 47, forming the elements do not distinguish over Chou et al. because only the final product/structure is relevant, not the process of forming the elements such as "photo processing/etching", "laser machining", "drilling" or "plasma processing". Note that a "product by process" claim is directed to the product per se, no matter how actually made, In re Hirao, 190 USPQ 15 at 17 (footnote 3). See also In re Brown, 173 USPQ 685; In re Luck, 177 USPQ 523; In re Fessmann, 180 USPQ 324; In re Avery, 186 USPQ 161; In re Wertheim, 191 USPQ 90 (209 USPQ 554 does not deal with this issue); and In re Marrosi et al., 218 USPQ 289, all of which make it clear that it is the patentability of the final product per se which must be determined in a "product by process" claim, and not the patentability of the process, and that an old or obvious product produced by a new method is not patentable as a product, whether claimed in "product by process" claims or not . Note that applicant has the burden of proof in such cases, as the above case law makes clear. See also MPEP 706.03(e).

Regarding claim 48, Chou et al. teach substantially the entire claimed structure as applied to claim 47, wherein Chou et al. teach the semiconductor die being wire bonded to the respective plurality of conductive pads on the conductive portions (see wire bonds

1026a, 1026b, etc. in Fig. 10A).

Regarding claim 51, Chou et al. teach substantially the entire claimed structure as applied to claim 47 above, wherein Chou et al. teach the conductive layer (512/1011a-1011d in Fig. 10A/10B) having an opening in a central portion for attaching/bonding the die to the substrate (see Fig. 10A).

Regarding claim 52, Chou et al. disclose a semiconductor component/assembly/package (1000 in Fig. 10A/10B; Col. 16, lines 5-21) comprising:
- a substrate made of material such as a printed circuit board (PCB), plastic/epoxy laminate, ceramic, etc. (not numerically referenced in Fig. 10A/10B- Col. 1, line 53, Col. 10, line 29, Col. 16, line 46) having top and bottom surfaces
- a conductive layer (512/1011a-1011d in Fig. 10A/10B) having elements/land segments comprising a plurality of conductive portions including first portions (1011a and 1011d in Fig. 10A/10B) and second portions (1011b and 1011c in Fig. 10A/10B),
- a plurality of conductors comprising first and second portions including conductive pads/sites (not numerically referenced- see bonding pads/sites on 1011a/1011d and 1011b/1011c respectively connected by bonding wires in Fig. 10A)
- the plurality of conductors having a size, a spacing and a shape defined by a plurality of recesses/grooves (not numerically referenced- see recesses/grooves

in Fig. 10A/10B) through the conductive layer, each first portion of the conductor being separated from an adjacent conductor by the groove/recess and the second portion of the conductor (see 1011a and 1011d being spaced from 1011b by a recess/groove in Fig. 10A/10B)

- a semiconductor die (die 502 in Fig. 10A/10B) being wire bonded on the top surface of the substrate in an electrical communication with the conductors comprising conductive portions/conductive pads

- a plurality of electrically conductive vias through the substrate (1034a, 1034b, etc. in Fig. 10A/10B) in electrical communication with the conductors (1011a, 1011b, etc. respectively in Fig. 10A), and

- a plurality of external contacts/balls (not numerically referenced in Fig. 10A- see 5223-522e in Fig. 5B; Col.16, lines 46-53) in a ball grid array (BGA) on the bottom surface of the substrate, the external contacts/balls being in electrical communication with the respective conductive vias and conductive portions of the conducive layer (Col. 16, lines 33-38)

(Fig. 10A/10B; Fig. 5A-5G; Col. 16, line 5- Col. 17, line 15).

Chou et al. fail to teach the conductive metal layer substantially covering the surface of the substrate and the plurality of first and second portions of the conductive layer being configured for signal transmission and being not configured for signal transmission respectively.

Chou et al. further teach in another embodiment (Fig. 11A/11B), the conductive layer being extended to include a thermally and an electrically conductive die attach/paddle metal area (Col. 17, lines 16-50), the die attach/paddle metal area being selectively connected with one or more of the land segment/pad region of the first or second portions of the conductive layer to provide a significant increase in the area covering the surface of the substrate and to provide the enhanced thermal dissipation and heat transfer from the die (Col. 17, lines 50-65). Furthermore, such land/pad connections comprise one or more grounded/non-signal transmission electrical connections (see Col. 17, lines 30-50).

It would have been obvious to a person of ordinary skill in the art at the time invention was made to incorporate the conductive metal layer substantially covering the surface of the substrate and the plurality of first and second portions of the conductive layer being configured for signal transmission and being not configured for signal transmission respectively as taught by Chou et al. in the embodiment of Fig. 11A/11B so that the thermal dissipation and electrical performance/grounding can be improved in Chou et al's component.

Regarding claim 52, forming the elements do not distinguish over Chou et al. because only the final product/structure is relevant, not the process of forming the elements such as "photo processing/etching", "laser machining", "drilling" or "plasma processing". Note

that a "product by process" claim is directed to the product per se, no matter how actually made, In re Hirao, 190 USPQ 15 at 17 (footnote 3). See also In re Brown, 173 USPQ 685; In re Luck, 177 USPQ 523; In re Fessmann, 180 USPQ 324; In re Avery, 186 USPQ 161; In re Wertheim, 191 USPQ 90 (209 USPQ 554 does not deal with this issue); and In re Marrosi et al., 218 USPQ 289, all of which make it clear that it is the patentability of the final product per se which must be determined in a "product by process" claim, and not the patentability of the process, and that an old or obvious product produced by a new method is not patentable as a product, whether claimed in "product by process" claims or not . Note that applicant has the burden of proof in such cases, as the above case law makes clear. See also MPEP 706.03(e).

Regarding claim 53, Chou et al. teach substantially the entire claimed structure as applied to claim 25, wherein Chou et al. teach the plurality of external contacts/balls (not numerically referenced in Fig. 10A- see 522a, 522b, etc. in Fig. 5B; Col. 10, lines 35-70, Col.16, lines 46-53) on the substrate in electrical connection with the conductive vias (1036a-1036d in Fig. 10B, Col. 16, lines 33-38).

3. Claims 27 and 34 are rejected under 35 U.S.C. 103(a) as being unpatentable over Chou et al. (US Pat. 5691568) in view of Pedder (US Pat. 5717245).

Regarding claim 27, Chou et al. teach substantially the entire claimed structure as applied to claim 25, except the die being flipchip mounted to the conductors.

Pedder teaches a BGA package having multichip module (MCM) where chips are electrically connected to conductive potions of the substrate using conventional configurations including a wire bonding connection (43 in Fig. 2) and flipchip mounting connections (41/42 in Fig. 2., Col. 4, lines 43-49).

It would have been obvious to a person of ordinary skill in the art at the time invention was made to incorporate the die being flipchip mounted to the conductors as taught by Pedder so that the dimensions of the conductive pads can be reduced and the chip density and electrical performance can be can be improved in Chou et al's component.

Regarding claim 34, Chou et al. teach substantially the entire claimed structure as applied to claim 30, except an encapsulant at least partially covering the die and a portion of the surface.

Pedder teaches using a sealant/encapsulant to encapsulate the BGA package/module (Col. 1, line 55).

It would have been obvious to a person of ordinary skill in the art at the time invention was made to incorporate the encapsulant covering the die and a portion of the surface as taught by Pedder so that the surface protection for the electrical connections can be improved and the damage from contamination and moisture can be reduced in

Chou et al's component.

4. Claim 38 is rejected under 35 U.S.C. 103(a) as being unpatentable over Chou et al. (US Pat. 5691568) in view of Beaman et al. (US Pat. 5531022).

Regarding claim 38, Chou et al. teach substantially the entire claimed structure as applied to claim 35, wherein Chou et al. further teach the substrate comprising an insulating layer on the surface (not numerically referenced in Fig. 10A- see 506a in Fig. 5A-5C; Col. 10, line 23., Col. 16, line 21), but Chou et al. fail to teach the substrate comprising a semiconductor material.

Beaman et al. teach using a high performance package (2 in Fig. 1) having a multilayered substrate (MLS) where the substrate (8 in Fig. 1) comprises an insulating layer and a semiconductor material such as silicon (Col. 3, line 48) to improve thermal conductivity (Col. 3, lines 45-52).

It would have been obvious to a person of ordinary skill in the art at the time invention was made to incorporate the substrate comprising the semiconductor material as taught by Beaman et al. so that the thermal dissipation and electrical performance can be improved in Chou et al's component.

5. Claims 49 and 50 are rejected under 35 U.S.C. 103(a) as being unpatentable over Chou et al. (US Pat. 5691568) in view of Rostoker et al. (US Pat. 618101 1).

Regarding claims 49 and 50, Chou et al. teach substantially the entire claimed structure as applied to claim 47 above, wherein Chou et al. further teach using a reduced pitch between the lands/pads and using shorter bonding wires to provide reduced impedance and improved manufacturing yield and reliability (Col. 16, lines 55-37), but Chou et al. fail to teach each conductor or each groove having a first width and a second width of about 5 microns respectively.

Rostoker et al. teach using a semiconductor component in a variety of packages including a BGA package where wiring/conductor dimensions such as width (W), spacing/groove size (S), thickness (T), etc. (Fig. 4, Col. 9, lines 15-20) are optimized in order to reduce the capacitance and interconnect delay and to improve the speed and package performance (Col. 9, line 15- Col. 10, line 30). Furthermore, the width (W) and space/groove (S) dimensions have a range of values including a range of 0.16-20 microns for the width dimension and a ratio W/S being in a range of 0.7-1.0 (Col. 10, lines 5-20, see W and W/S values and ratios listed in Table in Col. 10).

It would have been obvious to a person of ordinary skill in the art at the time invention was made to incorporate each conductor or each groove having a first width and a second width of about 5 microns as taught by Rostoker et al. so that the capacitance and interconnect delay can be reduced and the speed/performance of the package can be improved in Chou et al's component.

Response to Arguments

6. Applicant's arguments filed on 01-12-04 have been fully considered but they are not persuasive.

A. Applicant contends that there is no suggestion of laser machining the conductive elements in Chou et al.

However, the examined claims are directed to a device/component structure and not to a method of forming the conductive elements in the component. Therefore, Chou et al's structure comprising the first and second portions of the conductive layer is applied for the above rejections.

B. Applicant contends that the conductive portions including the land/pad and the die pad areas in Chou et al. do not separate adjacent traces as recited in the amended claims.

However, the embodiment in Fig. 11A/11B of Chou et al. teaches the conductive layer being extended to include a thermally and an electrically conductive die attach/paddle metal area (Col. 17, lines 16-50), the die attach/paddle metal area being selectively connected with one or more of the land segment/pad region of the first or second portions of the conductive layer. It would have been obvious to one of ordinary skill in the art to recognize that such selective/separated land/pad connections would provide the desired number of grounded/non-signal transmission electrical connections

for the respective conventional connecting elements such as pads, traces, landings, etc. (see Col. 17, lines 30-50).

Conclusion

7. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Nitin Parekh whose telephone number is 571-272-1663. The examiner can normally be reached on 09:00AM-05:30PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Lee can be reached on 571-272-1732. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9318.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-308-0956.

Nitin Parekh

NP
04-02-04

Primary Examiner
Steve Lee